R09

Code No: D109110608

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.Tech I Semester Regular Examinations March/April 2010

CPLD& FPGA ARCHITECTURES AND APPLICATIONS

(COMMON TO DSCE, WIRELESS & MOBILE COMMUNICATION, VLSI SYSTEM DESIGN/VLSI/VLSI DESIGN, COMMUNICATION SYSTEMS, EMBEDDED SYSTEMS & VLSI DESIGN, VLSI & EMBEDDED SYSTEMS)

Time: 3hours **Max.Marks:60**

Answer any five questions

All questions carry equal marks

- - -

1. (a). Draw and explain architecture of PLD.

   (b). With diagram explain Functional block.

2. (a). Explain Architecture of Altera MAX 5000 series CPLD.

   (b). Explain the ACT 2 and ACT 3 Logic Modules.

3. (a). Draw and explain the General Block diagram of FPGA.

   (b). Discuss Speed performance of different FPGAs.

4. (a). Write short note on extended Petri nets for parallel controllers.

   (b). Explain about One Hot State machine.

5. (a). Explain Basic concepts of Petri nets for state machines.

   (b). Explain briefly about Front end Design tools for ASICs.

6. Explain in detail about Design flow using FPGAs.

7. (a). Explain about Parallel Adder Cell.

   (b). Briefly explain about Serial Multiplier with Parallel Addition.

8. Write short notes on any TWO of the following:

   (i). EDA tools

   (ii).Speed performance of different CPLDs.

   (iii).Applications of CPLDs

****